Design of a 250 MS/s 8-bit Current-Steering DAC in 0.18 µm CMOS

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I. Introduction

This report presents the design of a 250 MS/s 8-bit digital-to-analog converter (DAC) in a 0.18 µm CMOS technology with a 1.8 V supply. The DAC targets wireline transmitter applications and must deliver at least 1.5 $V_{pp,diff}$ into a 100 Ω differential transmission-line load, with spurious-free dynamic range (SFDR) exceeding 48 dB across the Nyquist band. Key static specifications include DNL $< \pm 1$ LSB and INL $< \pm 2$ LSB. Each bit weight must be independently tunable over a $\pm 10\%$ range via 6-bit trim DACs.

II. Architecture

A. Current-Steering Topology

A current-steering architecture is chosen for its inherent DNL/INL and speed improvement: output current is steered between a differential pair switch. This ensures that the shared source node of the differential pair maintains a constant voltage, which guarantees that a current switch is saturated as a DAC bit is asserted, which prevents the output from drooping due to current inrush to charge the previously discharged node. A droop at such a high sampling frequency would introduce significant static error and thus degrade our DNL, INL performance. This makes it well-suited to the 250 MS/s sample rate. We also choose to implement a current switch scaling scheme on each unit current cell in order to limit V_{DS} mismatches.

B. Segmentation: 3-bit Thermometer MSBs + 5-bit Binary LSBs

The 8-bit input word is split into 3 MSBs and 5 LSBs. The 3 MSBs are thermometer-encoded via a 3-to-7 binary-to-thermometer decoder, producing 7 unit-weighted control signals. The 5 LSBs remain binary-weighted, controlling current sources scaled at $1\times$, $2\times$, $4\times$, $8\times$, and $16\times$ the unit current I_u.

This 3+5 segmentation is chosen for the following reasons:

- **Glitch energy reduction at MSB transitions.** Thermometer coding of the 3 MSBs ensures that each MSB code step activates (or deactivates if counting down) exactly one unit current cell. The worst-case glitch transition in the thermometer section is limited to the activation of just one thermometric unit cell, with the overall worst-case glitch transition being when one such thermometric cell is activated and all of the binary cells turn off.
- **Reduced decoder complexity.** Our implementation of a 3-to-7 thermometer decoder requires only 11 logic gates (not counting any driving inverters). As we scale the thermometer bits, the number of logic gates increases drastically (a 5-to-31 decoder required by a 5-MSB thermometer scheme), reducing digital area, power, and routing complexity substantially if laid out.

A 2+6 split (2 thermometer MSBs, 6 binary LSBs) was considered but provides only 3 thermometer cells, offering minimal glitch improvement. A 4+4 split improves linearity further with 15 thermometer cells but increases decoder and latch complexity substantially for diminishing returns at 8 bits. The chosen 3+5 split represents a practical compromise between dynamic linearity and implementation complexity for this design.

C. Signal Path Overview

The signal flow through the DAC is as follows:

1) The 8-bit unsigned input is split into D[7:5] (MSBs) and D[4:0] (LSBs).
2) A 3-to-7 binary-to-thermometer decoder converts the 3 MSBs into 7 thermometer-coded unit-cell control signals.
3) The 5 LSBs drive binary-weighted current switches directly (weights $1\times$, $2\times$, $4\times$, $8\times$, $16 \times I_u$).
4) All 12 switch-control signals (7 thermometer + 5 binary) pass through retiming latches clocked on the rising edge of CLK_T (250 MHz), ensuring all switches transition simultaneously and minimising code-dependent glitches.
5) The retimed signals drive differential NMOS switch pairs that each steer unit currents to the output nodes.
6) The differential output drives the 100 Ω transmission-line load through on-chip 50 Ω termination resistors on each side, with 550 fF parasitic pad/ESD capacitance to ground at each output.

D. Analog Weight Tuning

Each of the 12 current cells (7 thermometer + 5 binary) includes an independent 6-bit binary-weighted trim DAC. The trim DAC injects or subtracts a small current I_{trim} at the common-source node between the cascode and

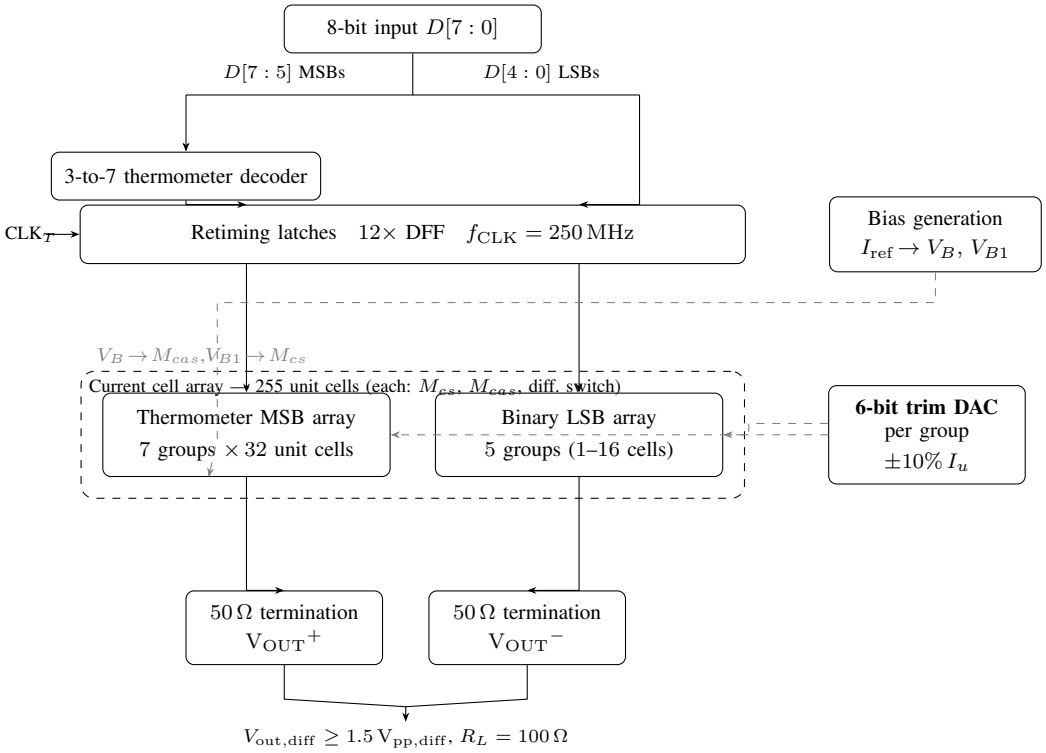


Fig. 1. Block diagram of the 8-bit 3+5 segmented current-steering DAC. Solid arrows: signal flow. Dashed arrows: bias/control distribution. Each of the 12 cell groups includes an independent 6-bit trim DAC for post-fabrication mismatch correction ($\pm 10\%\, I_u$).

main current-source transistors, adjusting the effective cell weight by $\pm 10\%$. For the binary LSB cells, accurate weight ratios ($1:2:4:8:16$) are important for monotonicity within each thermometer step; the trim DACs allow post-fabrication correction of random mismatch without requiring layout-level calibration.

III. Building Block Design

A. Unit Current Cell

The unit current cell is the core building block, replicated 7 times for the thermometer MSB section and scaled (by $1\times$, $2\times$, $4\times$, $8\times$, $16\times$) for the 5 binary LSB cells. It consists of, from bottom to top: a main current-source NMOS (M_{cs}), a cascode NMOS (M_{cas}), and a differential switch pair (M_{sw+}, M_{sw-}).

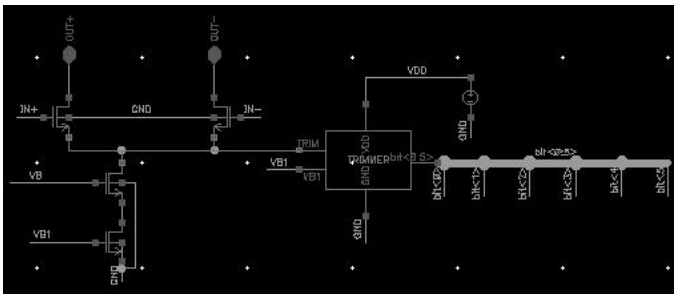


Fig. 2. Schematic of a Unit Current Source

1) Unit Current Determination: The full-scale differential output voltage is

$$V_{\mathrm{out,diff}} = (2^N - 1) \cdot I_u \cdot R_{\mathrm{load}} \tag{1}$$

where $N = 8$, $R_{\mathrm{load}} = 100\,\Omega$ (differential), and the specification requires $V_{\mathrm{out,diff}} \geq 1.5\,\mathrm{V_{pp}}$, corresponding to a single-ended peak swing of $\pm 750\,\mathrm{mV}$ at each output node. Since the differential output is formed by two complementary half-swings, the full-scale current steered to a single output side is $255 \cdot I_u$, and the peak single-ended voltage is $255 \cdot I_u \cdot R_{\mathrm{term}}$ where $R_{\mathrm{term}} = 50\,\Omega$. Setting this equal to 750 mV:

$$I_u = \frac{0.75\,\mathrm{V}}{255 \times 50\,\Omega} \approx 58.8\,\mu\mathrm{A} \tag{2}$$

We round up to $I_u = 60\,\mu\mathrm{A}$, yielding a full-scale differential swing of $2 \times 255 \times 60\,\mu\mathrm{A} \times 50\,\Omega = 1.53\,\mathrm{V_{pp}}$.

2) Current Source Sizing for Mismatch: The dominant static-linearity limitation is random mismatch between unit current sources. For the thermometer-coded MSB section, the DNL at any unit-cell transition equals the normalised current error of the switching cell:

$$\mathrm{DNL_{thermo}} = \frac{\Delta I_u}{I_{\mathrm{LSB}}} = \frac{\Delta I_u}{I_u} \cdot 2^5 = \frac{\Delta I_u}{I_u} \cdot 32 \tag{3}$$

since each unit thermometer cell carries I_u and one LSB of the full 8-bit DAC equals $I_u/32$ (the binary LSB section has 5 bits, so one LSB $= I_u/2^5$). For DNL $< \pm 1$ LSB at 3σ yield this requires:

$$3\,\frac{\sigma(I_u)}{I_u} \cdot 32 < 1 \quad \Longrightarrow \quad \frac{\sigma(I_u)}{I_u} < \frac{1}{96} \approx 1.04\% \tag{4}$$

For the binary LSB section, the worst-case carry transition (code 15→16 within each thermometer step) switches the $16\times I_u$ cell on while the four lower cells ($1\times$ through $8\times$, totalling $15\times I_u$) switch off. The net current error is the sum of independent mismatch contributions from all five binary cells. Since each $k\times$ cell has absolute current variance $\sigma^2(k\,I_u) = k^2\,\sigma^2(I_u)$ (for cells sized with $W \propto k$, $\sigma(I)/I$ is constant, so $\sigma(k\,I_u) = k\,\sigma(I_u)$), the total 3σ error at the midscale carry is:

$$3\,\sigma_{\text{carry}} = 3\,\sigma(I_u)\sqrt{16^2+8^2+4^2+2^2+1^2} \approx 55.4\,\sigma(I_u) \tag{5}$$

Requiring this to be less than $1\,\text{LSB} = I_u$ gives:

$$\frac{\sigma(I_u)}{I_u} < \frac{1}{55.4} \approx 1.81\% \tag{6}$$

The thermometer constraint (1.04%) is therefore the binding requirement. We adopt a conservative target of

$$\frac{\sigma(I_u)}{I_u} \le 1.0\% \quad (1\sigma) \tag{7}$$

Binary LSB cells are sized with $W \propto$ weight while keeping $L = 2\,\mu\text{m}$, maintaining the same $\sigma(I)/I$ per unit current.

The relative current mismatch has two contributions. Threshold voltage mismatch produces

$$\left.\frac{\sigma(I)}{I}\right|_{V_T} = \frac{g_m}{I_D}\cdot\frac{A_{V_T}}{\sqrt{WL}} \tag{8}$$

and β mismatch produces

$$\left.\frac{\sigma(I)}{I}\right|_{\beta} = \frac{A_\beta}{\sqrt{WL}} \tag{9}$$

where $A_{V_T} = 5\,\text{mV}\cdot\mu\text{m}$ and $A_\beta = 0.01\,\mu\text{m}$ are the technology mismatch parameters.

3) Overdrive Voltage Selection: The overdrive voltage $V_{OV} = V_{GS} - V_{TH}$ of the current-source transistor controls the trade-off between mismatch sensitivity and voltage headroom. In the square-law region, $g_m/I_D = 2/V_{OV}$.

A headroom analysis of the cascode stack determines the maximum allowable V_{OV}. From the 1.8 V supply, the voltage budget from ground to the switch-pair source node is

$$V_{DS,M_{cs}} + V_{DS,M_{cas}} \le V_{\text{out,min}} - V_{DS,\text{sw,min}} \tag{10}$$

The minimum output voltage occurs at full scale: $V_{\text{out,min}} = V_{DD} - I_{\text{FS}}\cdot R_{\text{term}} = 1.8 - 255\times 60\,\mu\text{A}\times 50\,\Omega = 1.418\,\text{V}$. Allowing $V_{DS,\text{sw,min}} \approx 150\,\text{mV}$ for the switch, the cascode stack can occupy up to $1.418 - 0.15 = 1.268\,\text{V}$.

With $V_{OV} = 200\,\text{mV}$ for both M_{cs} and M_{cas}, each device requires $V_{DS,\text{sat}} + V_{\text{margin}} \approx 300\,\text{mV}$, totalling 600 mV and leaving 668 mV of headroom margin.

4) Transistor Dimensions: With $V_{OV} = 200\,\text{mV}$, $g_m/I_D = 2/V_{OV} = 10\,\text{V}^{-1}$. The combined relative mismatch numerator is:

$$\sqrt{(g_m/I_D\cdot A_{V_T})^2 + A_\beta^2} = 0.0510\,\mu\text{m} \tag{11}$$

so the total relative current mismatch is:

$$\frac{\sigma(I)}{I} = \frac{0.0510}{\sqrt{WL}} \tag{12}$$

Setting $\sigma(I)/I \le 1.0\%$ requires:

$$\sqrt{WL} \ge \frac{0.0510}{0.01} = 5.10\,\mu\text{m} \quad\Longrightarrow\quad WL \ge 26.0\,\mu\text{m}^2 \tag{13}$$

The required W/L ratio follows from the square-law drain current:

$$I_D = \frac{\mu_n C_{ox}}{2}\cdot\frac{W}{L}\cdot V_{OV}^2 \tag{14}$$

Using $\mu_n C_{ox} = 2.066\times 10^{-4}\,\text{A/V}^2$ for the TSMC 0.18 µm process:

$$\frac{W}{L} = \frac{2\times 60\,\mu\text{A}}{2.066\times 10^{-4}\,\text{A/V}^2\times(0.2\,\text{V})^2} = \frac{60\times 10^{-6}}{8.264\times 10^{-6}} = 14.52 \tag{15}$$

Choosing $L = 2\,\mu\text{m}$ (long channel for improved matching and output resistance) gives $W = 14.52\times 2 = 29.04\,\mu\text{m}$. The resulting $WL = 58.08\,\mu\text{m}^2$ exceeds the minimum $26.0\,\mu\text{m}^2$ required for the $\sigma(I)/I \le 1.0\%$ target, yielding:

$$\frac{\sigma(I)}{I} = \frac{0.0510}{\sqrt{58.08}} = 0.67\% \quad\Rightarrow\quad 3\sigma = 2.01\% \tag{16}$$

This satisfies the binding thermometer DNL constraint ($\sigma(I_u)/I_u < 1.04\%$) with adequate margin. Binary LSB cells are sized with W scaled proportionally to their weight while keeping $L = 2\,\mu\text{m}$, so the largest LSB cell ($16\times$) has $W = 256\,\mu\text{m}$.

Table I summarises the current-source transistor parameters.

TABLE I
MAIN CURRENT SOURCE (M_{cs}) PARAMETERS

Parameter	Value
Unit current I_u	60 µA
Overdrive voltage V_{OV}	200 mV
$\mu_n C_{ox}$	$2.066\times 10^{-4}\,\text{A/V}^2$
W/L (unit / thermo cell)	16 µm / 2 µm
W/L (binary LSB $16\times$ cell)	256 µm / 2 µm
g_m/I_D	$10\,\text{V}^{-1}$
$\sigma(I)/I$ (1σ, unit cell)	0.67%
$3\sigma(I)/I$ (unit cell)	2.01%
DNL constraint (3σ)	$< 1.04\%$ (thermo, binding)
Min. WL for $\sigma \le 1.0\%$	$26.0\,\mu\text{m}^2$
Actual WL (unit cell)	$58.0\,\mu\text{m}^2$

B. Cascode Transistor (M_{cas})

1) Role and Motivation: The cascode transistor M_{cas} is inserted between the differential switch pair and the main

current source M_{cs}. Its gate is biased using a current mirror, so its source voltage is held approximately constant regardless of the output voltage swing. Without M_{cas}, the $\pm 750\,\text{mV}$ differential output swing would appear directly across $V_{DS,M_{cs}}$, modulating I_D through the CLM coefficient λ and producing signal-correlated current errors. Since these errors are deterministic and periodic, they generate harmonics rather than noise, directly degrading SFDR.

2) Output Impedance Requirement from SFDR: The 48 dB SFDR specification requires that the worst-case harmonic distortion component remain below $-48\,\text{dBc}$. The dominant mechanism linking output impedance to SFDR is the signal-dependent drain current variation of the current sources. For a single-tone output at frequency f_{out}, the third-order harmonic amplitude relative to the fundamental is approximately:

$$\text{HD3} \approx \frac{1}{4}\left(\frac{R_{\text{load}}/2}{r_{out,\text{total}}}\right)^2 \tag{17}$$

Setting HD3 $< -48\,\text{dBc}$ ($= 3.98 \times 10^{-3}$ in linear scale):

$$r_{out,\text{total}} > \frac{R_{\text{load}}/2}{2\sqrt{\text{HD3}}} = \frac{50}{2\sqrt{3.98 \times 10^{-3}}} \approx 396\,\Omega \tag{18}$$

This is the minimum combined parallel output impedance of all 255 unit cells seen at either output node. Per unit cell this requires:

$$r_{out,\text{cell}} > 396 \times 255 \approx 101\,\text{k}\Omega \tag{19}$$

3) Output Impedance Without Cascode: For M_{cs} alone with $L = 2\,\mu\text{m}$, the channel-length modulation coefficient is approximately $\lambda \approx 0.05\,\text{V}^{-1}$, giving:

$$r_{ds,M_{cs}} = \frac{1}{\lambda I_u} = \frac{1}{0.05 \times 60\,\mu\text{A}} \approx 667\,\text{k}\Omega \tag{20}$$

While this nominally exceeds the $101\,\text{k}\Omega$ requirement, it does not account for the signal-dependent variation of $V_{DS,M_{cs}}$ across the full $\pm 750\,\text{mV}$ output swing. The resulting CLM-induced current modulation is:

$$\frac{\Delta I}{I_u} = \lambda \cdot \Delta V_{DS} = 0.05 \times 1.5 = 7.5\% \tag{21}$$

This 7.5% signal-correlated error would produce harmonics far exceeding the $-48\,\text{dBc}$ SFDR requirement. The small-signal r_{ds} is therefore insufficient as a linearity metric; what matters is the effective impedance seen by the signal swing, which is drastically reduced by CLM modulation. A cascode is therefore necessary.

4) Output Impedance With Cascode: With M_{cas} inserted above M_{cs}, the drain of M_{cs} is decoupled from the output. The combined cascode output impedance is:

$$r_{out,\text{cascode}} \approx g_{m,cas} \cdot r_{ds,cas} \cdot r_{ds,cs} \tag{22}$$

With $g_m = g_m/I_D \times I_u = 10 \times 60\,\mu\text{A} = 600\,\mu\text{S}$ and $r_{ds} \approx 667\,\text{k}\Omega$ for both devices:

$$r_{out,\text{cascode}} \approx 600 \times 10^{-6} \times (667 \times 10^3)^2 \approx 133\,\text{G}\Omega \tag{23}$$

This far exceeds the $101\,\text{k}\Omega$ per-cell requirement, providing ample margin. The combined parallel impedance of all 255 cells is $133\,\text{G}\Omega/255 \approx 522\,\text{M}\Omega$, which is $\gg R_{\text{load}}/2 = 50\,\Omega$.

5) Sizing: M_{cas} is identically sized to M_{cs}: $W = 29.0\,\mu\text{m}$, $L = 2\,\mu\text{m}$, $V_{OV} = 200\,\text{mV}$ to carry the same current.

C. Differential Switch Pair

The switch pair (M_{sw+}, M_{sw-}) steers I_u between OUT+ and OUT−. Minimum channel length ($L_s = 360\,\text{nm}$) is used for maximum switching speed and minimum charge injection. Width is set to $W_s = 1.44\,\mu\text{m}$, sufficient to carry $I_u = 60\,\mu\text{A}$ in saturation. Gates are driven rail-to-rail (0 to 1.8 V) by the retiming latch outputs. We notice that a very large overdrive voltage on the current switches improves our SFDR. All 255 unit cells use identical switch dimensions.

D. Bias Generation

The cascode and current-source gate biases V_B and V_{B1} are generated by a diode-connected stack driven by a $60\,\mu\text{A}$ reference current I_2 from VDD. Two series diode-connected NMOS ($W = 29\,\mu\text{m}$, $L = 2\,\mu\text{m}$) set the bias voltages. The cascode bias is fixed at $V_B = 885\,\text{mV}$, which ensures M_{cas} remains in saturation while keeping M_{cs} in saturation with adequate headroom margin across the full output swing.

E. 6-bit Trim DAC

The goal of the trim DAC is to accept a user-defined 6-bit code and create a scaled compensation current based on it, assuming that the user knows the extent of the current mismatch (manual control). The trim DAC designed here can be encoded and applied to either each unit current cell individually or to all unit current cells that constitute one DAC bit, depending on the level of control that the user is assumed to have.

The trim DAC operates thermometrically by turning on up to five NMOS or five PMOS, which can each sink or source current respectively into a unit cell (with each MOS passing 2% of the unit cell's current for 10% overall correction). The choice of whether to use NMOS or PMOS is controlled by the sixth bit, which serves as a sign bit that turns on either the NMOS or the PMOS and turns off the other depending on the sign of the required correction. Its design is thermometric instead of binary, because this design avoids V_{DS} mismatch allows the MOS sizing to be fine-tuned such that each MOS can precisely provide 2% of the unit cell current. Binary implementations can often have V_{DS} mismatch and cannot have this fine-tuned sizing because there are multiple possible V_{DS} values to tune for when a given MOS turns on. Thermometric ensures that there is only one possible V_{DS} value to fine tune for in each MOS, that being the one time it turns on. This thermometric design sacrifices resolution (from 31 to 5 combinations) in order to ensure that DNL is not worsened due to V_{DS} changes affecting each MOS's compensation current.

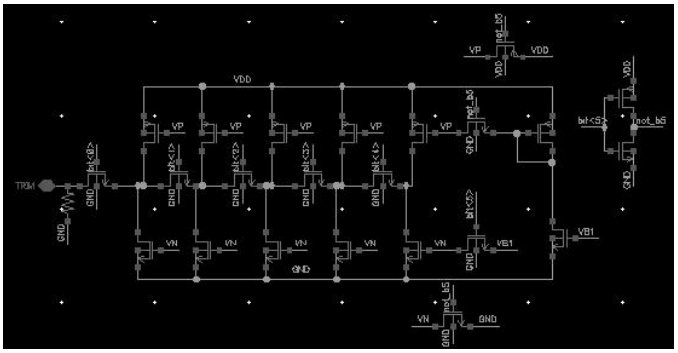


Fig. 3. Trimming DAC Schematic

F. Retiming Latches and Thermometer Decoder

All 12 switch-control signals pass through D flip-flops clocked on the rising edge of CLKT (250 MHz) before reaching the switch gates. Each flip-flop produces complementary outputs Q and $\overline{\text{Q}}$, which drive M_{sw+} and M_{sw-} directly. The 5 binary LSB bits and 7 thermometer MSB bits are retimed independently. By synchronising all 12 signals to the same clock edge, inter-switch timing skew is reduced from the combinational propagation delay spread ($\sim$50 ps) to the flip-flop output skew ($\sim$1–2 ps), suppressing code-dependent glitch energy and protecting SFDR.

The 3-to-7 binary-to-thermometer decoder converts the 3 MSBs D[7:5] into the 7 thermocode signals upstream of the retiming stage. Its implementation is shown in Fig. 4.

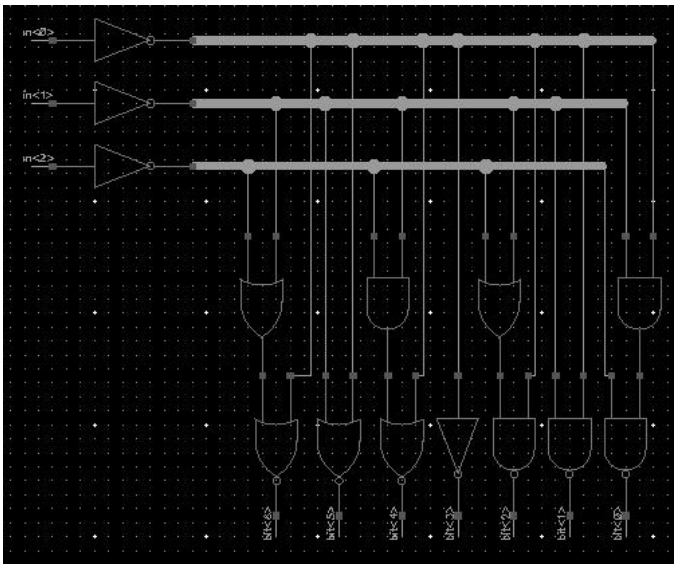


Fig. 4. Decoder Schematic

IV. DAC Design and Simulation

A. Static Performance

1) INL and DNL: The linearity characterization is based on the transient simulation output $V_{\text{OUT}}(t)$ exported from Cadence Virtuoso, in which the DAC sweeps through all 256 input codes over a 20.4 µs window (approximately 79.7 ns per code).

Since the data is time-domain rather than code-indexed, the 255 output transitions are first located by thresholding the discrete derivative of the waveform:

$$|V_{\text{OUT}}[n] - V_{\text{OUT}}[n-1]| > 0.3\,\text{mV} \tag{24}$$

Samples belonging to the same transition event are grouped together. The first detected event corresponds to a startup transient and is discarded. For each of the remaining 255 transitions, the step size w_k is measured as:

$$w_k = V_{\text{after}}^{(k)} - V_{\text{before}}^{(k)}, \quad k = 1, \ldots, 255 \tag{25}$$

where $V_{\text{before}}^{(k)}$ and $V_{\text{after}}^{(k)}$ are the output voltage computed over a 30-sample. For each transition, the settled output voltage is estimated by averaging samples taken well within the steady-state region of each code period, away from switching transients.

The ideal LSB voltage Δ is defined as the mean of all measured step sizes:

$$\Delta = \frac{1}{255} \sum_{k=1}^{255} w_k \tag{26}$$

Using the mean as the reference ensures that the DNL values sum identically to zero, which is consistent with the end-to-end definition of the transfer curve.

The DNL at each code transition k is:

$$\text{DNL}[k] = \frac{w_k}{\Delta} - 1, \quad k = 1, \ldots, 255 \tag{27}$$

A value of $\text{DNL}[k] = 0$ indicates a perfect step. Missing codes occur when $\text{DNL}[k] \leq -1$.

The INL is computed as the cumulative sum of the DNL, anchored at zero for code 0 (endpoint method):

$$\text{INL}[k] = \sum_{i=1}^{k} \text{DNL}[i], \quad k = 1, \ldots, 255 \tag{28}$$

This is equivalent to measuring the deviation of the actual transfer curve from the straight line connecting the first and last output levels, normalized to Δ.

The DNL and INL plots are shown below for the three corners. As can be seen in Figs. 5, 6, 7, by the INL plots, our DAC exhibits third-order nonlinearity as expected by a differential nature. Similarly, we do not observe any second order distortion. The DNL profile exhibits a characteristic parabolic envelope, with small negative values at the lower and upper code extremes and positive values toward midscale. This shape is a direct consequence of the binary-to-thermometer decoding scheme: the mean LSB used as reference is computed across all 255 transitions, so codes near the edges deviate slightly from this average, while transitions near midscale remain closest to it. In all three corners, the DNL remains well within $\pm 2 \times 10^{-4}$ LSB, confirming excellent static linearity.

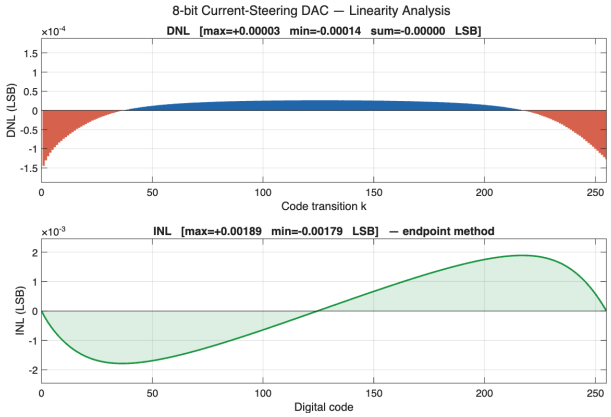


Fig. 5. DNL and INL plots over tt corner

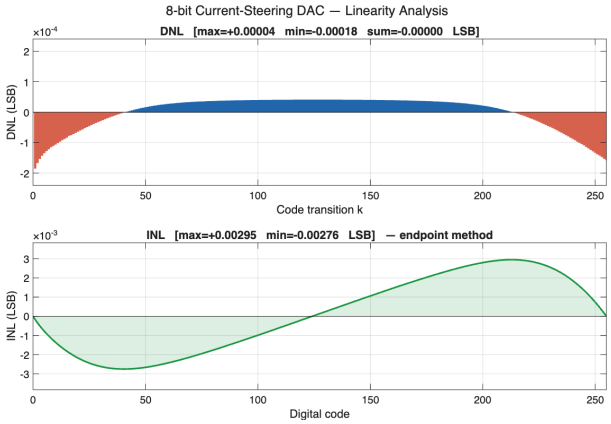


Fig. 6. DNL and INL plots over ff corner

2) Tuning Range Demonstration: To demonstrate the trimmer DAC's ability to linearly provide compensation current in a thermometric fashion, Figure 8 uses annotation to show how each additional input bit asserted provides a consistent 0.933μA additional current.

B. Dynamic Performance

Based on the DNL vs. code plot, the blocks that contribute most to DNL and thus INL and SFDR/SNDR are likely the thermometric DAC bits, as the DNL is highest in magnitude while they are transitioning.

As seen in Figs. 13, 14, and 15, the SFDR gets worse as input frequency increases. This is because the circuit will experience larger glitches (as shown in Figure 12) due to quicker switching exacerbating the effects of MOSFET capacitive parasitics. Eventually, J/M reaches Nyquist rate, and aliasing causes what we see as a beat frequency, which results in another form of distortion. An example of the non-beating transient performance is shown in Figure 10. An example of the beating transient performance is shown in Figure 11.

SFDR, SNDR, and ENOB values are also degraded in corners, as expected. In the FF corner, it was shown that the SFDR is below the requirement. However, as can be seen in Fig. 9, the raw FFT result shows that the SFDR at that corner is 51.5dB.

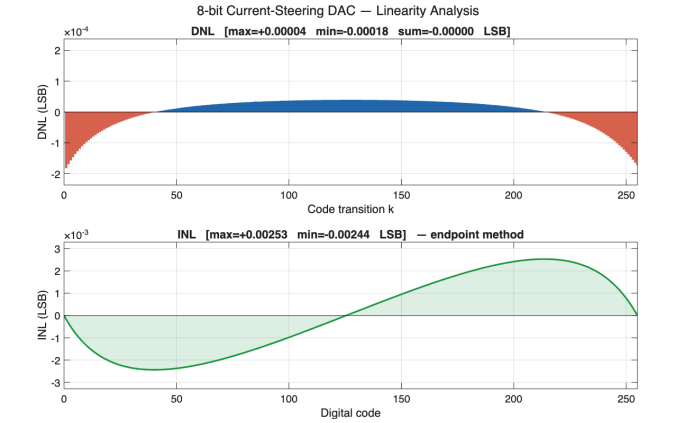


Fig. 7. DNL and INL plots over ss corner

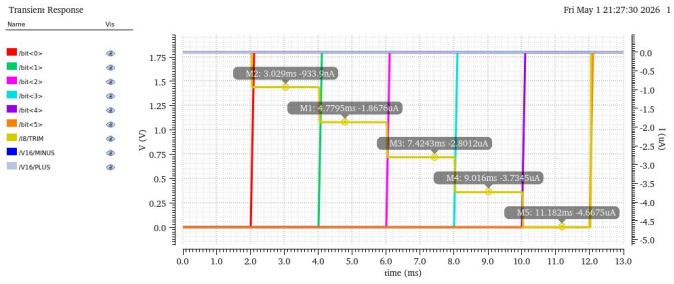


Fig. 8. Thermometric Trim Decoder Performance on a Unit Current Source

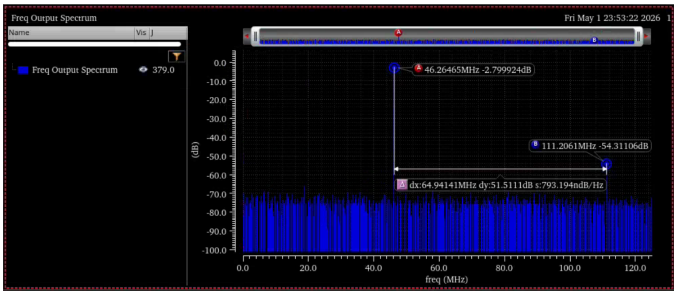


Fig. 9. FFT showing the SFDR on the SS corner

C. Performance Summary

Seen below in Table II is a summary of the performance of the DAC across the three process corners. Note that the power consumption for each block and the entire circuit was simply calculated using $V_{DD} \times I$ and measuring the supply current drawn for the respective circuit. The blocks are chosen as such since the complete DAC bits are simply parallel-connected power-of-2 multiples of the unit cell (so their power consumption is as well).

TABLE II
DAC PERFORMANCE SUMMARY ACROSS PROCESS CORNERS

Parameter	**SS**	**TT**	**FF**
$\lvert DNL\rvert_{max}$	1.8×10^{-4} LSB	1.4×10^{-4} LSB	1.8×10^{-4} LSB
$\lvert INL\rvert_{max}$	2.53×10^{-3} LSB	1.89×10^{-3} LSB	2.95×10^{-3} LSB
ENOB (low freq.)	5.5 bits	7.93 bits	5.5 bits
ENOB (Nyquist)	7.9 bits	7.90 bits	7.9 bits
SFDR (low freq.)	60 dB	66.5 dB	60 dB
SFDR (Nyquist)	61 dB	66 dB	61 dB
SNDR (low freq.)	34 dB	49.5 dB	35 dB
SNDR (Nyquist)	49.5 dB	49.3 dB	49 dB
Power Breakdown			
Trim DAC	$8.40\,\mu W$ $(3.04 \times 10^{-2}\%)$	$7.77\,\mu W$ $(2.81 \times 10^{-2}\%)$	$7.79\,\mu W$ $(2.82 \times 10^{-2}\%)$
Unit Cell	$116.4\,\mu W$ (0.39%)	$115.8\,\mu W$ (0.38%)	$115.8\,\mu W$ (0.38%)
Inverter	$5.75\,pW$ $(2.08 \times 10^{-5}\%)$	$31.05\,pW$ $(1.12 \times 10^{-4}\%)$	$326.52\,pW$ $(1.18 \times 10^{-3}\%)$
Total Power	$27.666\,mW$	$27.648\,mW$	$27.648\,mW$

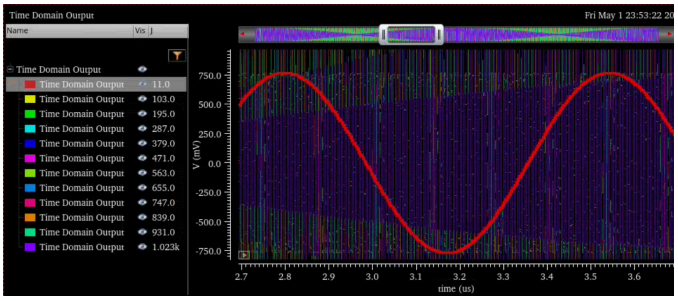


Fig. 10. Non-beating example, at 1.3 MHz input frequency

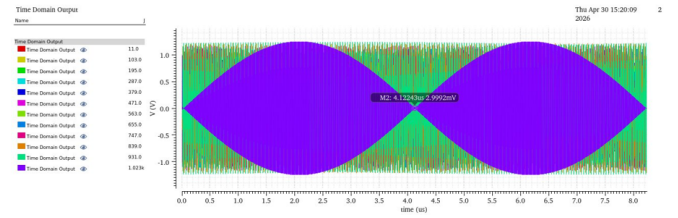


Fig. 11. Beating example, at an input frequency at the edge of the Nyquist rate

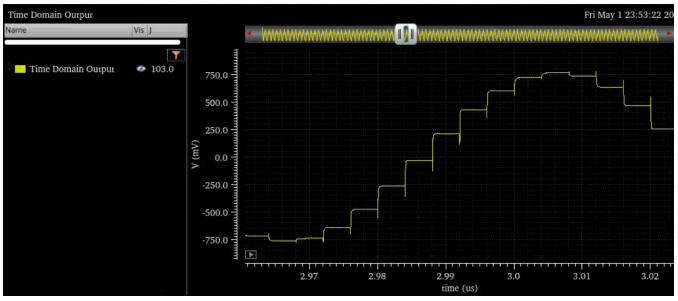


Fig. 12. Glitches at DAC transitions

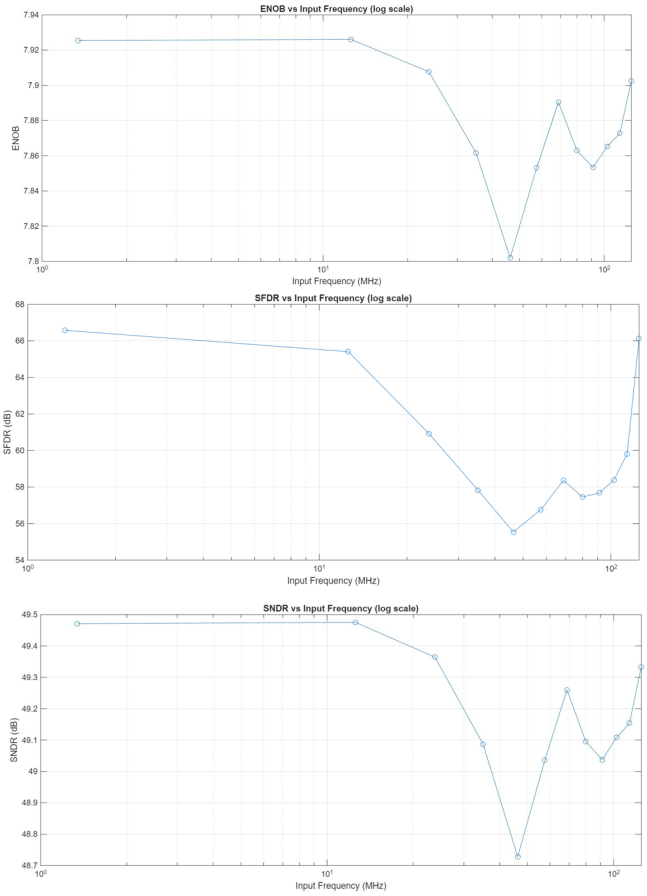


Fig. 13. ENOB, SFDR and SNDR for the TT corner

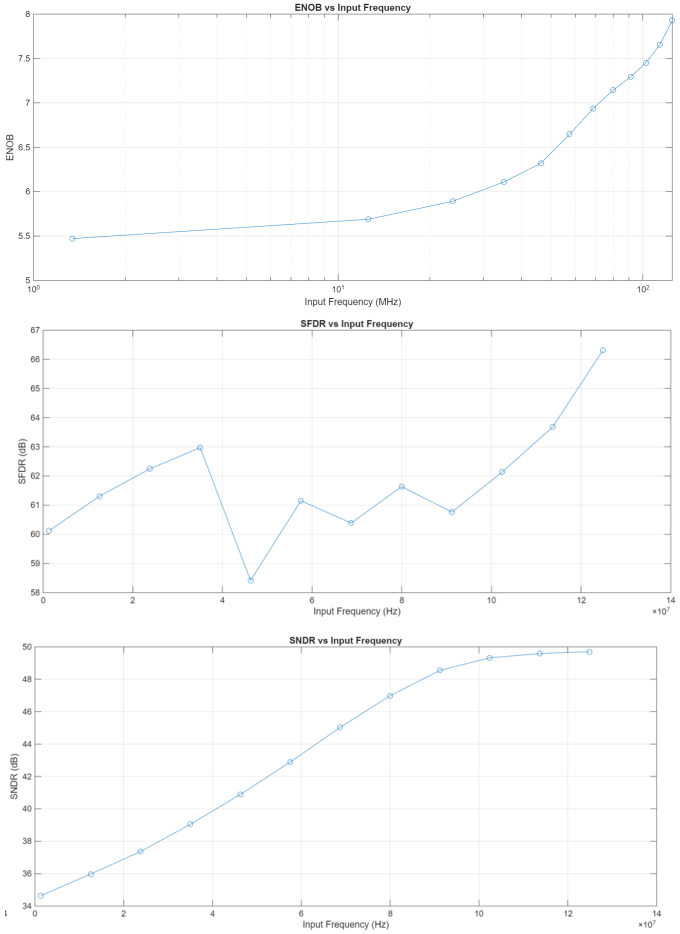


Fig. 14. ENOB, SFDR and SNDR for the SS corner

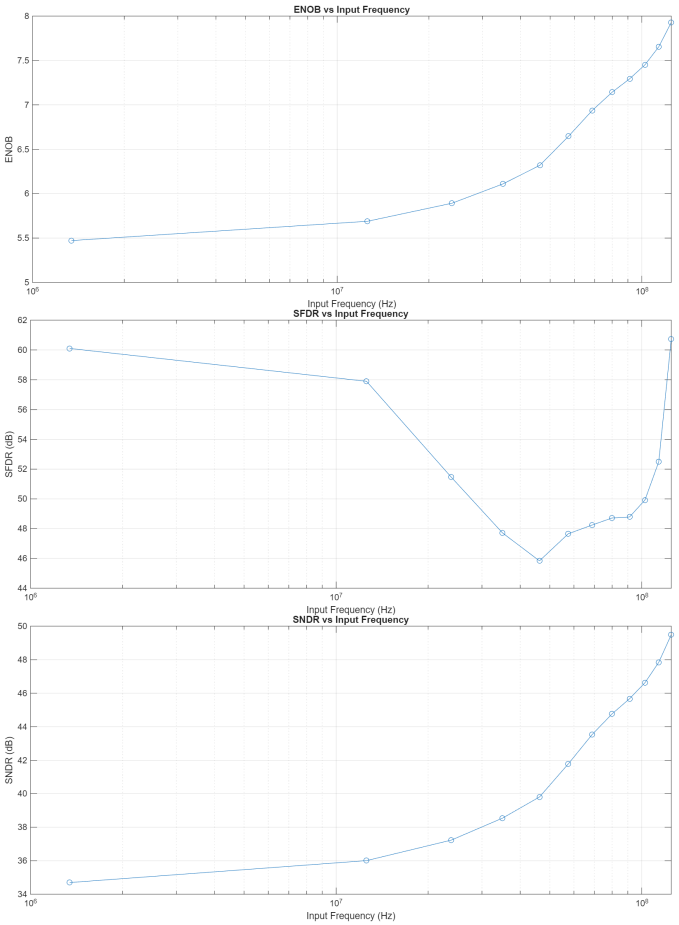


Fig. 15. ENOB, SFDR and SNDR for the FF corner