Design of a Fully Differential Switched-Capacitor Amplifier in CMOS 0.18 μm Technology

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INTRODUCTION

This report presents the design of a fully differential switched-capacitor sample-and-hold amplifier with a nominal gain of 2, intended for use as the residue amplification stage in a pipelined ADC. The circuit is implemented in TSMC 0.18 µm CMOS with a 1.8 V supply, targeting a sampling frequency of 16 MHz and an overall ADC resolution of 7 bits.

The core of the design is a folded-cascode OTA, chosen for its ability to achieve high DC gain and wide output swing within the constrained supply voltage, while maintaining a single dominant pole that simplifies frequency compensation.

I. SYSTEM-LEVEL DESIGN

A. Full-Scale Voltage, Common-Mode Voltage, and LSB Size

The supply voltage is $V_{DD} = 1.8\,\text{V}$ (TSMC 0.18 µm process). To keep all switches and the OTA output stage well within the supply rails, we bound the input range by one overdrive voltage $V_{ov} = 0.2\,\text{V}$ from each rail:

$$V_{in,\min} = V_{ov} = 0.2\,\text{V}, \qquad V_{in,\max} = V_{DD} - V_{ov} = 1.6\,\text{V}$$

Common-mode voltage. The common-mode voltage is chosen at the midpoint of the input range:

$$V_{CM} = \frac{V_{in,\max} + V_{in,\min}}{2} = \frac{1.6 + 0.2}{2} = 0.9\,\text{V}$$

This choice maximizes headroom symmetrically for a fully differential design and keeps both NMOS and PMOS switches reasonably on across the full signal swing.

Full-scale voltage. The differential full-scale voltage spans the entire usable input range:

$$V_{FS} = V_{in,\max} - V_{in,\min} = 1.6 - 0.2 = 1.4\,\text{V}$$

LSB size. For an $N = 7$-bit converter, the voltage corresponding to one least significant bit is:

$$V_{LSB} = \frac{V_{FS}}{2^N - 1} = \frac{1.4}{2^7 - 1} = \frac{1.4}{127} \approx 11\,\text{mV}$$

B. Switched-Capacitor Input Stage

In a sampled-data system, the thermal noise of the switch on-resistance is sampled onto the capacitor every clock cycle. The resulting noise power (referred to the capacitor voltage) is:

$$\overline{V_{n,RMS}^2} = \frac{kT}{C_{samp}}$$

where k is Boltzmann's constant and T is absolute temperature. To ensure the sampling noise does not significantly degrade the converter's resolution, we impose:

$$V_{RMS}^2 < \frac{V_{LSB}^2}{24}$$

Substituting $V_{LSB} \approx 11\,\text{mV}$ and solving at $T = 300\,\text{K}$:

$$C_{samp} > \frac{24\,kT}{V_{LSB}^2} = \frac{24 \times 1.38 \times 10^{-23} \times 300}{(11 \times 10^{-3})^2} \approx 0.821\,\text{fF}$$

This sets only a lower bound. We choose:

$$\boxed{C_{samp} = 150\,\text{fF} = 0.15\,\text{pF}}$$

This value is selected based on the following considerations:

- **Thermal noise margin.** The chosen value is more than two orders of magnitude above the minimum, providing substantial margin against kT/C noise.
- **Settling speed and slew rate.** The time constant of the sampling network scales as $\tau = \frac{2}{3} R_{on} C_{samp}$. A

larger capacitor requires a wider switch (lower R_{on}) or a longer settling time. Keeping C_{samp} moderate relaxes the slew rate requirement on the OTA, since the peak current needed to charge the capacitor scales as $I_{slew} = C_{samp} \cdot SR$.

- **Parasitics.** In a 0.18 µm process, junction and routing parasitics are on the order of femtofarads. Choosing $C_{samp} = 0.15\,\text{pF}$ ensures that parasitic capacitances remain a small fraction of the signal capacitance, preserving the accuracy of the charge transfer and the designed transfer function.
- **High-frequency noise aliasing.** A larger capacitor presents a lower impedance at high frequencies, but the noise bandwidth of the R_{on}–C_{samp} network is $f_n = 1/(\frac{2}{3}R_{on}C_{samp} \times 2\pi) = \frac{3}{4\pi R_{on}C_{samp}}$. Choosing C_{samp} too small widens this noise bandwidth and increases the amount of out-of-band thermal noise folded back into the signal band upon sampling.
- **Power consumption.** The dynamic power drawn to charge and discharge the capacitor each cycle scales as $P = C_{samp}V_{FS}^2 f_s$. Keeping $C_{samp} \leq 0.15\,\text{pF}$ limits this contribution at $f_s = 16\,\text{MHz}$ to an acceptable level.
- **Area.** On-chip MIM or MOM capacitors in 0.18 µm occupy area proportional to their value. At 0.15 pF the capacitor remains compact and does not dominate the layout.

The circuit operates in two non-overlapping clock phases, ϕ_s (sampling) and ϕ_h (hold/amplification). The analysis is carried out on the positive half of the fully differential circuit; the negative half is symmetric.

During ϕ_s, the sampling capacitor C_{samp} is connected between V_{in}^+ and the OTA input node V_{OTA}^-, while the feedback capacitor C is reset. The OTA input voltage (referred to common mode) is:

$$V_{OTA}^+ = V_{in}^+ - V_{CM}, \qquad V_{OTA}^- = V_{in}^- - V_{CM}$$

The charge stored on each sampling capacitor is therefore:

$$Q^+ = 2\,C_{samp}\,V_{OTA}^+, \qquad Q^- = 2\,C_{samp}\,V_{OTA}^-$$

The total differential charge sampled is:

$$Q_{tot} = 2\,C_{samp}\big(V_{OTA}^+ - V_{OTA}^-\big) = 2\,C_{samp}\big(V_{in}^+ - V_{in}^-\big)$$

During ϕ_h, the bottom plate of C_{samp} is switched to V_{CM} and the feedback capacitor C closes the loop around the OTA. For an ideal OTA (infinite DC gain), the virtual ground forces V_{OTA}^+ to converge towards V_{CM}.

The charge on the positive node is now:

$$Q^+ = \big(V_{OTA}^+ - V_{CM}\big)\,C_{samp} + \big(V_{out}^+ - V_{OTA}^+\big)\,C_{samp}$$

$$Q^+ = C_{samp}\big(V_{out}^+ - V_{CM}\big)$$

Similarly,

$$Q^- = -C_{samp}\big(V_{out}^- - V_{CM}\big)$$

The total differential charge in this phase is:

$$Q_{tot} = Q^+ + Q^- = C_{samp}\big(V_{out}^+ - V_{out}^-\big) = C_{samp}\,V_{out,\,diff}$$

Applying charge conservation between ϕ_s and ϕ_h:

$$Q_{tot,\,\phi_s} = Q_{tot,\,\phi_h}$$

$$2\,C_{samp}\,V_{in,\,diff} = C_{samp}\,V_{out,\,diff}$$

$$\boxed{V_{out,\,diff} = 2\,V_{in,\,diff}}$$

The switched-capacitor gain block therefore implements a differential gain of **2**, set purely by the capacitor ratio and independent of the OTA's absolute gain (provided the DC gain is sufficiently large).

At a sampling frequency of $f_s = 16\,\text{MHz}$, one full clock period is:

$$T_{clk} = \frac{1}{f_s} = 62.5\,\text{ns}$$

Each clock phase ϕ_s and ϕ_h ideally receives half of this, i.e. 31.25 ns. Accounting for the non-overlap dead time between the two phases, the usable settling window is conservatively:

$$t_{settle} \approx 28\,\text{ns}$$

The output must settle to within half an LSB of its final value. The required relative settling accuracy is therefore:

$$\epsilon = \frac{V_{LSB}/2}{V_{FS}} = \frac{11/2}{1400} \approx 0.393\%$$

For a first-order R_{on}–C_{samp} network, the settling error decays as $e^{-t/\tau}$. Imposing the accuracy requirement:

$$e^{-t_{settle}/\tau} < \frac{V_{LSB}}{2\,V_{FS}} = 0.00393$$

Taking the natural logarithm of both sides:

$$\frac{t_{settle}}{\tau} > -\ln(0.00393) \approx 5.54$$

$$\tau = \frac{2}{3}R_{on}\,C_{samp} < \frac{t_{settle}}{5.54} = \frac{28\,\text{ns}}{5.54} \approx 5.05\,\text{ns}$$

With $C_{samp} = 0.15\,\text{pF}$, the maximum allowable switch on-resistance is:

$$R_{on,\,max} = \frac{3\tau_{max}}{2C_{samp}} = \frac{1.5 \times 5.05\,\text{ns}}{0.15\,\text{pF}} = 50.5k\,\Omega$$

The on-resistance of a MOSFET switch in the linear region is:

$$R_{on_{n,p}} = \frac{1}{\mu_{n,p}C_{ox}\frac{W}{L}V_{ov}}$$

With the channel length fixed at $L = 1\mu\text{m}$ (to minimize short channel effects), the required width is:

$$W_n > \frac{L}{\mu_n C_{ox}\,(V_{GS} - V_{th})\,R_{on,\,max}} = 0.22\mu m$$

$$W_p > \frac{L}{\mu_p C_{ox}\left(V_{SG} - |V_{th}|\right) R_{on,\,max}} = 1.4\mu m$$

Through a test simulation for technology characterization we find: $\mu_n C_{ox} = 450\mu A/V^2$ & $\mu_p C_{ox} = 71.5\mu A/V^2$.

This is solved once the gate drive voltage $V_{GS} - V_{th}$ is 0.2V, as established from the supply and signal swing.

In order to maintain symmetry, we need the same R_{on} for both the NMOS and the PMOS devices in the switch pair. For that reason, we kept lengths of 180 nm, width of 571 nm for NMOS devices, and a width of 3.6 μm for PMOS devices.

Two additional non-ideal effects must be considered when sizing the switches:

- **Charge injection.** When a MOSFET switch turns off, the channel charge $Q_{ch} = WLC_{ox}(V_{GS} - V_{th})$ is partially injected onto C_{samp}, causing a voltage error $\Delta V = Q_{ch}/(2\,C_{samp})$. This error must remain below $V_{LSB}/2$, which places an upper bound on W (opposite to the R_{on} constraint). The two constraints together define a feasible window for W.
- **Clock feedthrough.** The gate-to-channel overlap capacitance $C_{ov} = W\,C'_{ov}$ couples the clock transition ΔV_{clk} directly onto the sampling node. The resulting error $\Delta V = C_{ov}\,\Delta V_{clk}/C_{samp}$ scales with W and is mitigated by using a fully differential topology (common-mode errors cancel) and by keeping W as small as R_{on} constraints permit.

A schematic of the differential switch is given in Fig. 1.

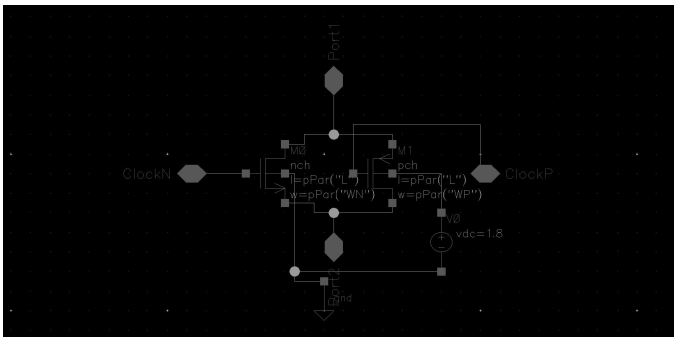


Fig. 1. Differential switch schematic

C. OTA Parameters

The OTA specifications are derived from the settling requirements established in Section A. We require the output to settle to within $V_{LSB}/2$ of its final value within the allotted time budget of $t_{settle} = 28\,\text{ns}$, for a full-scale differential input step of $\Delta V_{out} = V_{FS} = 1.4\,\text{V}$.

The feedback factor for this topology is:

$$\beta = \frac{C_{samp}}{C_{samp} + C_{samp}} = \frac{1}{2}$$

and the required relative settling accuracy is:

$$\epsilon \equiv \frac{V_{LSB}}{2\,V_{FS}} = \frac{11\,\text{mV}}{2 \times 1400\,\text{mV}} = 0.00393 = \frac{1}{2(2^N - 1)}$$

The closed-loop gain error of a feedback amplifier with open-loop gain A and feedback factor β is:

$$\text{Gain error} = \frac{1}{1 + A\beta}$$

Imposing that this error remain below the required accuracy ϵ:

$$\frac{1}{1 + A\beta} < \frac{V_{LSB}}{2\,V_{FS}}$$

$$\implies A > \left(\frac{2\,V_{FS}}{V_{LSB}} - 1\right)\frac{1}{\beta} = (2(2^N - 1) - 1)\,\frac{1}{\beta}$$

Substituting $N = 7$ and $\beta = 1/2$:

$$A > (254 - 1) \times 2 = 506 \implies \boxed{A_{min} \approx 54\,\text{dB}}$$

The input signal bandwidth of a sampled system is fundamentally limited by the Nyquist criterion to at most half the sampling frequency:

$$f_{sig} \leq \frac{f_s}{2} = \frac{16\,\text{MHz}}{2} = 8\,\text{MHz}$$

This is a constraint on the *input* signal, not on the OTA bandwidth, which must be set far higher to ensure adequate settling within t_{settle}.

For a single-pole closed-loop system, the output settles as $e^{-t/\tau_{cl}}$, where $\tau_{cl} = 1/(2\pi f_u \beta)$ and f_u is the open-loop unity-gain frequency. Imposing the settling condition:

$$e^{-\omega_u \beta\, t_{settle}} < \frac{V_{LSB}}{2\,V_{FS}}$$

$$\implies \omega_u \beta\, t_{settle} > \ln\left(\frac{2\,V_{FS}}{V_{LSB}}\right) = \ln(254) \approx 5.54$$

$$f_u > \frac{5.54}{2\pi\,\beta\,t_{settle}} = \frac{5.54}{2\pi \times 0.5 \times 28\,\text{ns}} \approx 63\,\text{MHz}$$

This is a **lower bound** valid only for an ideal single-pole system. Any additional poles (unavoidable in a real OTA) will degrade settling, so the true requirement on f_u will be higher. This figure is therefore a necessary but not sufficient condition. We will hence choose a minimum $f_u = 72MHz$ as a target unity gain bandwidth.

To avoid slewing distortion at the maximum operating frequency, the slew rate must exceed the maximum rate of change of a full-scale sinusoidal output of peak amplitude $V_p = V_{FS}/2 = 0.7\,\text{V}$:

$$SR \geq 2\pi\, f_u\, V_p = 2\pi \times 72\,\text{MHz} \times 0.7\,\text{V} \approx 317\,\text{V/µs}$$

The required tail current follows from $SR = I_{tail}/C_{load}$, where $C_{load} = 2\,C_{samp} = 0.3\,\text{pF}$:

$$I_{tail} = SR \times C_{load} = 317\,\text{V/µs} \times 0.3\,\text{pF} = 95\,\mu\text{A}$$

Finally, since we have a single pole system, one can expect a phase margin of 90°. However, consider the effect of a second pole as shown below:

$$PM = 180 - \arctan(\frac{f_u}{f_{fp1}}) - \arctan(\frac{f_u}{f_{p2}})$$

$$PM = 180 - \arctan(A_{OL}) - \arctan(\frac{f_u}{f_{p2}})$$

With A_{OL} being large, one expects $PM \leq 90°$ as we can expect a second pole due to parasitic capacitances as is typical of a folded cascode.

II. Transistor-level Design

A. Folded Cascode Topology

A folded cascode architecture was selected for the OTA implementation. The DC gain requirement of 54 dB is achievable in a single stage, eliminating the need for a two-stage design and the associated stability and power overhead. The folded cascode provides high output impedance through cascoding, which is necessary to meet the gain requirement, while offering better output swing than a telescopic cascode since the input pair and cascode devices do not share the same current branch. The circuit schematic is shown in Fig. 2.

B. Common Mode Feedback (CMFB)

The output common mode voltage must be stabilised at $V_{CM} = 0.9\,\text{V}$ independently of the differential signal. A switched-capacitor CMFB circuit is used, as it is well suited to the switched-capacitor environment of this design.

The CMFB circuit operates by sensing V_{out}^{+} and V_{out}^{-} directly at the gates of M14 and M15, which are biased in deep triode and therefore act as voltage-controlled resistors. This allows the sensed common mode to modulate the feedback current continuously and linearly. The W/L ratio of these transistors was determined by sweeping $V_{out,CM}$ against W/L, parametrized by V_{REF}. The chosen curve was the one that crossed V_{CM} with the lowest gradient (most immune to fluctuations in input common-mode offset). The sweep confirmed that $V_{out,CM} = V_{DD}/2 = 0.9\,\text{V}$ is achieved at $W/L = 7.49$ with $V_{REF} = 0.9\,\text{V}$.

The sizing of the remaining CMFB transistors is constrained by the mirroring conditions. M11 carries the tail current I_{tail} and is mirrored from I_{ref} via M12, with $W_{12} = W_{11}$. The condition:

$$W_{13} = W_{14} + W_{15}$$

ensures that when $V_{out,CM} = V_{REF}$, the current through M11 equals I_{ref}:

$$I_{D11} = I_{ref} \quad \text{when} \quad V_{out,CM} = V_{REF}$$

guaranteeing the OTA is biased at the correct operating point at equilibrium. All transistor sizes are summarised in Table I.

A schematic of the full high-level schematic is given in Fig. 3. The small blocks are switches while the large block is the OTA.

C. OTA Performance

The theoretical DC gain of our folded cascode OTA is given by:

$$A_{DC} = g_{m1}\left[((g_{m8} + g_{mb8})r_{o8}r_{o10})//((g_{m6} + g_{mb6})r_{o6}(r_{o4}//r_{o2}))\right]$$

where $g_{mb8} = 119.476\mu S and g_{mb6} = 100.304\mu S$.

TABLE I
Transistor sizes and small-signal parameters.

Transistor	W (μm)	L (μm)	g_m (μS)	r_o (kΩ)
M1, M2	5.27	1	367.8	827.9
M3, M4	66.42	1	689.1	11.28
M5, M6	33.21	1	392.9	466.9
M7, M8	5.27	1	391.0	476.0
M9, M10	5.27	1	357.8	27.86
M11, M12	10.54	1	795.3	247.2
M13	14.98	1	212.8	493.0
M14, M15	7.49	1	91.69	966.0

This yields an open-loop gain of $A_{DC} = 695 = 56.8$ dB.

From Fig. 5, one notices that the DC gain is 56.64 dB which is extremely close to its theoretical value. As can also be expected, $f_{p1} = \frac{f_u}{A_{DC}}$. Since we targeted $f_u = 72$ MHz, we expect $f_{p1} \approx 104$ kHz. Notice from Fig. 5, that $f_u = 84$ MHz and $f_{p1} = 130$ kHz, both being very close to their respective predicted values.

In addition, the folded cascode features a second pole resulting from capacitive parasitics located on the source node of the cascoding MOSFET (M5 for example, though M6 is equally valid due to symmetry). This pole's frequency is theoretically given by:

$$f_{p2} = \frac{g_{m5}}{2\pi C_X}$$

where C_X is the total capacitance on the cascode node. Taking the left side of the schematic (see Fig. 2), there is:

$$C_X = C_{gd1} + C_{db1} + C_{db3} + C_{gd3} + C_{gs5} + C_{sb5}$$

The values of the above quantities were found, in fF, to be: C_{gd1} = 1.92, C_{db1} = 3.385, C_{db3} = 76.09, C_{gd3} = 32.88, C_{gs5} = 201.6, and C_{sb5} = 83.85. This yields C_X = 399.725 fF, hence f_{p2} = 189.13 MHz based on the theoretical g_{m5}. In Fig. 4, one also observes a second pole at 246 MHz which once again confirms our expectations.

Fig. 5 shows the simulated open-loop common-mode gain. The DC common-mode gain is $A_{cm,0} \approx -276.7\,\text{dB}$, giving a CMRR of $333.4\,\text{dB}$, a direct consequence of the fully-differential, symmetric topology, which inherently suppresses common-mode signals at the output. This confirms excellent common-mode rejection across the entire signal band.

D. Benchmark Simulations

To perform benchmark simulations on the OTA and the high-level circuit, two testbenches were created. Fig. 6 shows the OTA testbench, while Fig. 7 shows the high-level testbench. For OTA simulations, a load of $2\times C_{samp} = 300fF$ was added to each output to simulate the loading of the OTA in the high-level circuit.

When benchmarking the OTA performance, a step function of V_{LSB} is applied to the inputs with V_{CM} set as the bias point. The output, shown in Fig. 8, has some capacitance charging due to parasitic capacitance, with an output that reaches near the maximum and minimum levels set by V_{FS}

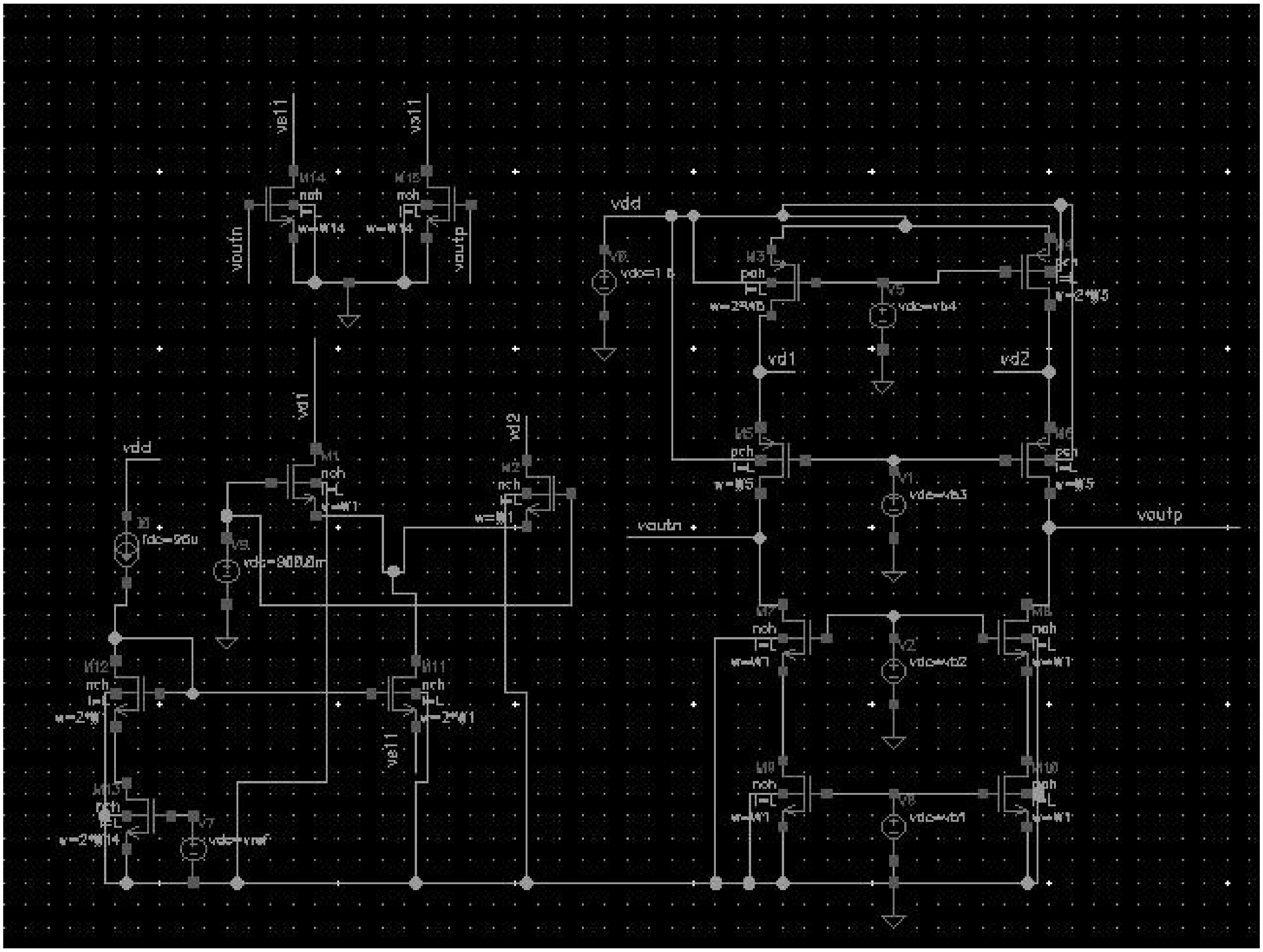


Fig. 2. OTA Schematic

and V_{OV} since DC gain is 679. Fig. 9 shows a similar scenario with capacitance charging, with the limiting of output if a step of amplitude V_{FS} is applied. Fig. 10 and 11 show the V_{FS} and V_{LSB} being applied as a step function in common-mode respectfully.

III. Performance Summary

A. Settling Error

To measure settling error, the step function is used with a magnitude of V_{LSB} as a differential input. This can be seen in Fig. 12. Once the step function rises to a non-zero value, a pulsing pattern can be seen where the output stabilizes to 2 times the V_{LSB} within 28 ns during the on time of the hold clock, and drops in magnitude during the on time of the sample clock. This may at first seem to be problematic, but it is a intentional design aspect for the device, as only the value during the hold period will be used in an ADC implementation. Since the output varies significantly from out expected output during the sampling period, the frequency dependency of gain for the device must be measured using a special technique called PAC, which will essentially takes set periodic measurements to be used for AC analysis. Overall, the output is able settle to significantly less than half the V_{LSB}.

B. Gain Error

Fig. 13 shows the simulated closed-loop differential gain. The DC gain is $5.9958\,\mathrm{dB}$ against an ideal of $6.0206\,\mathrm{dB}$ ($2\times$), giving a static gain error of

$$\epsilon_g = \frac{G_{\mathrm{ideal}} - G_{\mathrm{sim}}}{G_{\mathrm{ideal}}} = \frac{2 - 1.9943}{2} \approx 0.2856\,\% \qquad (1)$$

which is within the design specification of $\epsilon_{g,\,\mathrm{max}} = 0.393\,\%$, with a margin of $27.3\,\%$ relative to the budget. The $-3\,\mathrm{dB}$ closed-loop bandwidth is $f_{-3\,\mathrm{dB}} = 167\,\mathrm{MHz}$, confirming that the gain remains flat and well within specification across the entire signal band of interest.

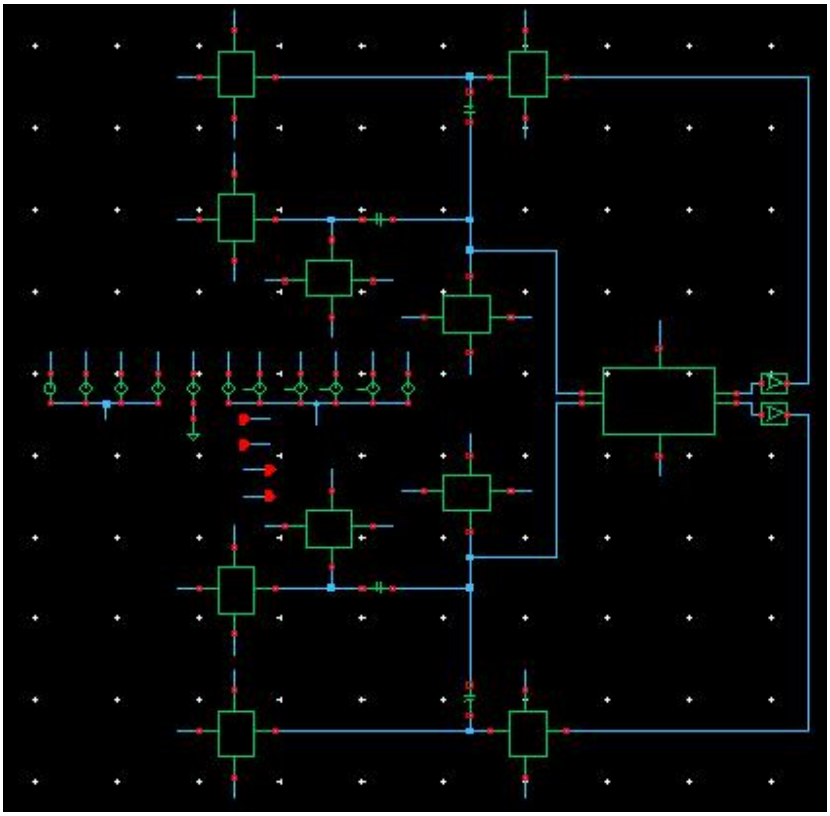


Fig. 3. Full high-level circuit schematic

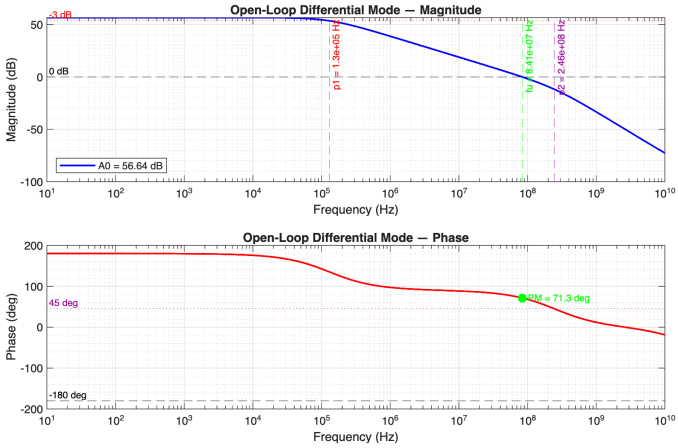


Fig. 4. Open-loop differential mode response

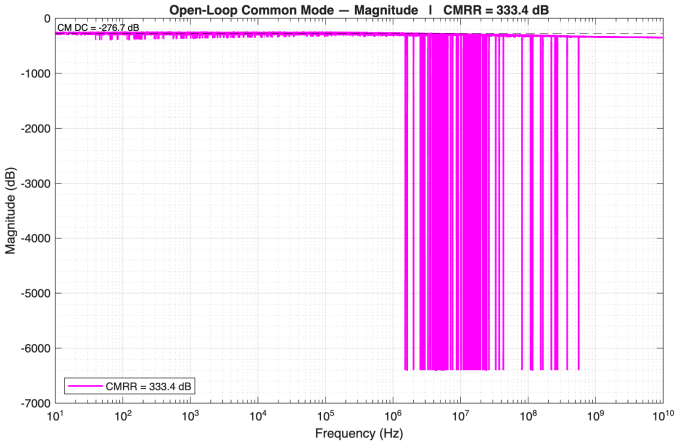


Fig. 5. Open-loop common mode response

C. Bandwidth and Phase Margin

The theoretical phase margin is given by

$$PM = 180 - \arctan(A_0) - \arctan\left(\frac{f_u}{f_{p2}}\right) \approx 180^\circ - 89.92^\circ - 20.85^\circ = 69.2^\circ \tag{2}$$

using $A_0 = 695$, $f_u = 72\,\text{MHz}$, and $f_{p2} = 189\,\text{MHz}$. From Fig. 14, the simulated value of $PM = 71^\circ$ agrees closely, with the small discrepancy attributable to higher-order parasitics. This phase margin value is also confirmed by Fig. 4 on which we observe $PM = 71.3^\circ$. A gain margin of $GM = 33.1\,\text{dB}$ further confirms robust stability. As expected, the loop-gain unity-gain frequency $f_{u,LG} = 99.8\,\text{MHz}$ matches the closed-loop $-3\,\text{dB}$ bandwidth, consistent with standard feedback theory.

D. Power Consumption and Figure of Merit

Total current consumption: $270.4\mu A$ Total power consumption: $486.72\mu W$ The Figure of Merit is hence $FoM = 2.3766 \times 10^{-13} = 0.23766$ pJ/step

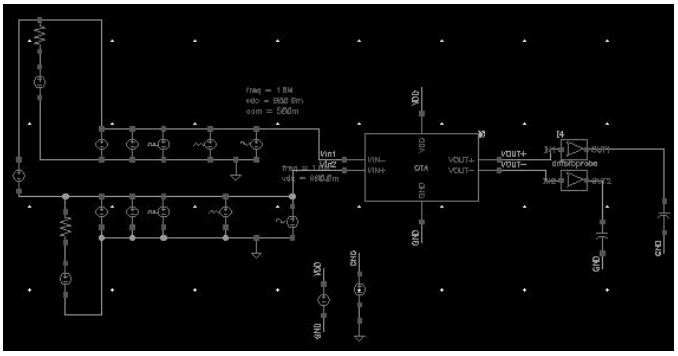


Fig. 6. Testbench for the isolated OTA

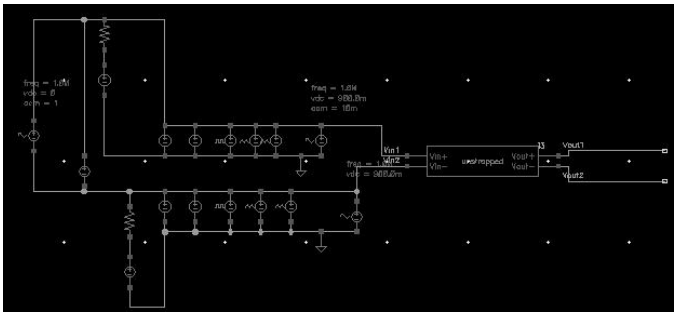


Fig. 7. Testbench for the high-level circuit

E. Differential Mode Step and Ramp Response

Shown in Fig. 15 and Fig. 16 are the V_{FS} step response and ramp response respectively using differential mode inputs. Since both inputs rise to V_{FS}, the outputs will be cutoff near V_{FS} since gain of 2 is no longer possible. The issue of dropping voltage within the output of the step function is simply due to the device switching to the sampling period as mentioned previously.

F. Overall Device Characteristic

Table II summarizes the performance and key parameters and metric in our design, showcasing all requirements being met.

TABLE II
OVERALL DEVICE CHARACTERISTIC/PARAMETERS.

Item	Value	Units
V_{FS}	1.4	V
Closed-Loop DC Gain	56.64	dB
Settling Error	0.09	%
Gain Error	0.2856	%
Phase Margin	69.2	Degrees
Gain Margin	33.1	dB
Closed-Loop 3dB Bandwidth	167	Mhz
V_{LSB}	11	mV
Total Current Consumption	270.4	μA
Total Power Consumption	486.72	μW
FOM	0.23766	pJ/step

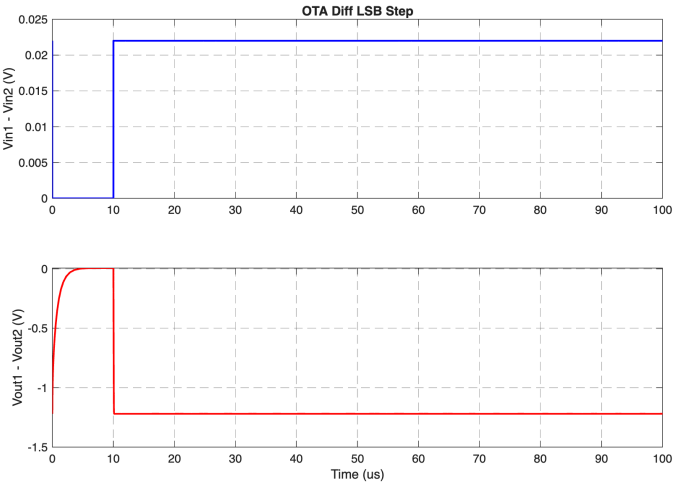


Fig. 8. OTA Differential LSB Step

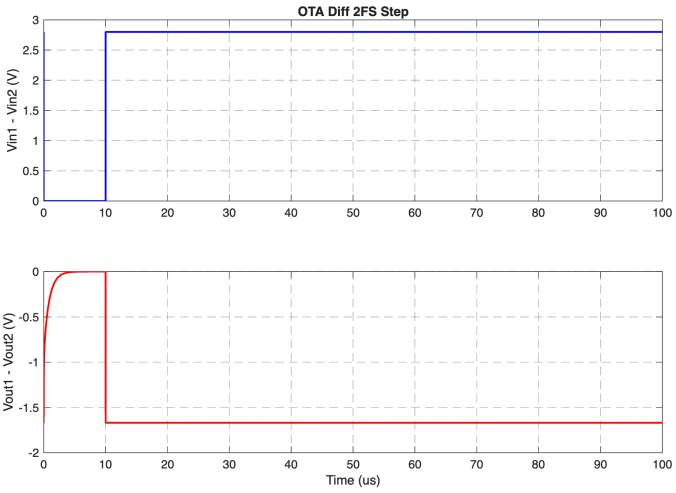


Fig. 9. OTA Differential FS Step

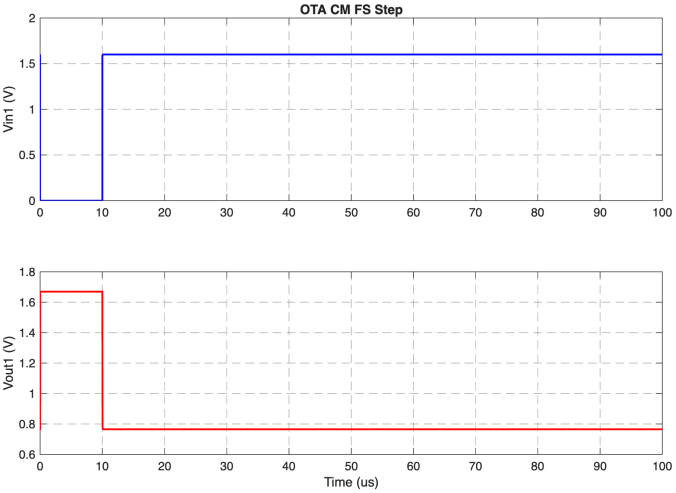


Fig. 10. OTA Common-Mode FS Step

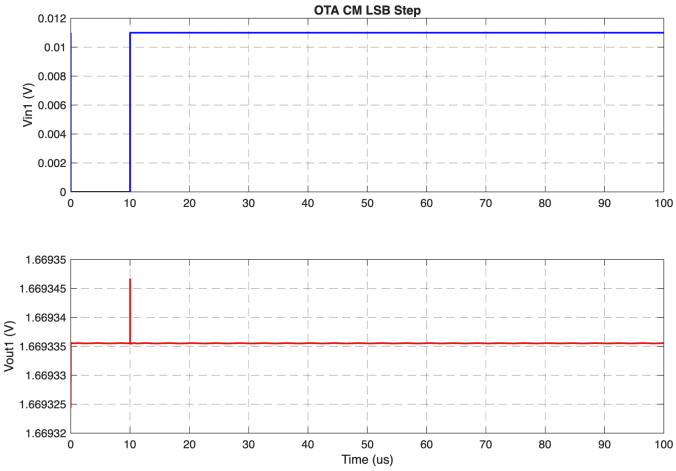


Fig. 11. OTA Common-Mode LSB Step

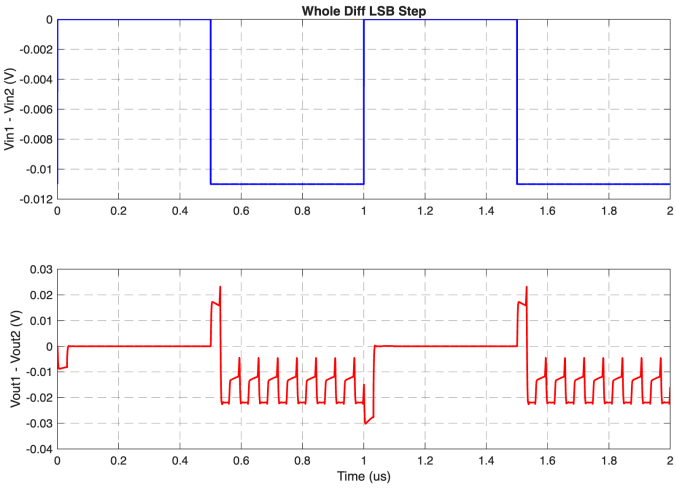


Fig. 12. Closed-loop LSB Step Transient

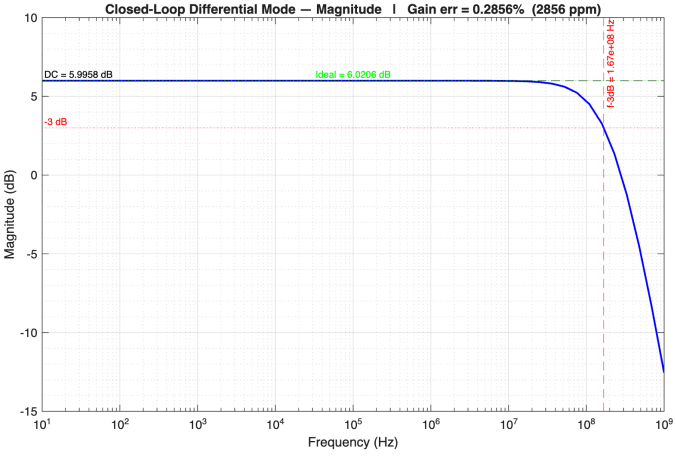


Fig. 13. Closed-Loop Differential Mode Response

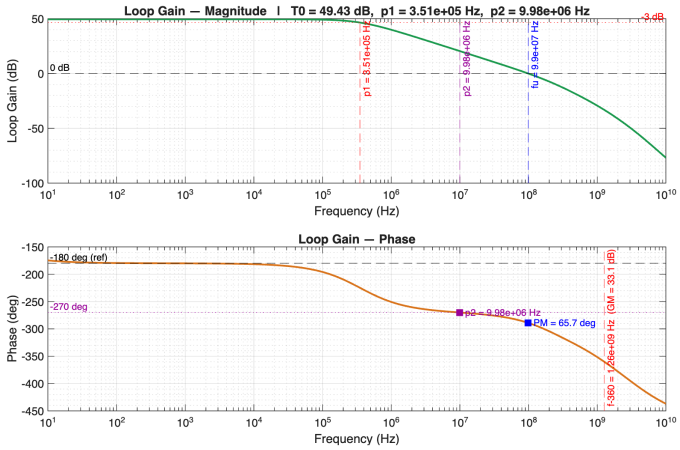


Fig. 14. Loop Gain Magnitude and Phase Plots

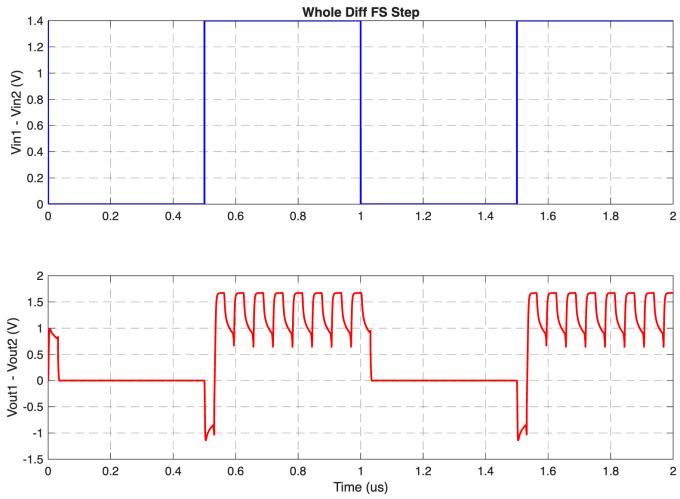


Fig. 15. Closed-looped Differential FS Step

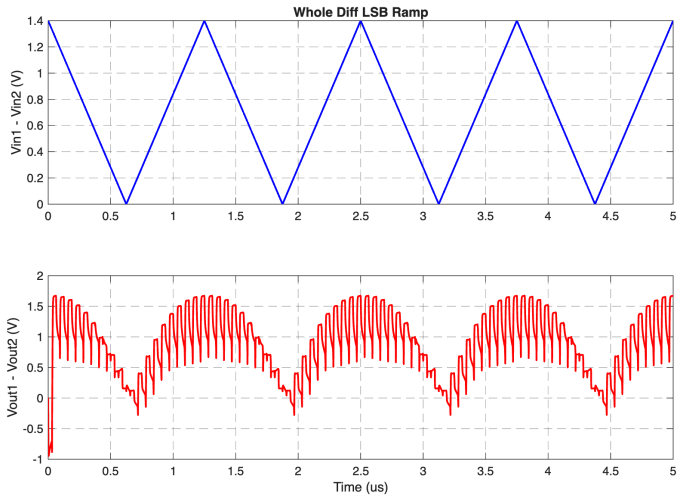


Fig. 16. Closed-looped Differential FS Ramp